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Brynjolfson, I.; Zilic, Z.;  
Custom Integrated Circuits Conference, 2000. CICC. Proceedings of the IEEE 2000  
21-24 May 2000 Page(s):139 - 142  
Digital Object Identifier 10.1109/CICC.2000.852635  
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- ☐ 2. **Asynchronous processor survey**  
Werner, T.; Akella, V.;  
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Volume 30, Issue 11, Nov. 1997 Page(s):67 - 76  
Digital Object Identifier 10.1109/2.634866  
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(352 KB\)](#) IEEE JNL
- ☐ 3. **Router plugins: a software architecture for next-generation routers**  
Decasper, D.; Dittia, Z.; Parulkar, G.; Plattner, B.;  
Networking, IEEE/ACM Transactions on  
Volume 8, Issue 1, Feb. 2000 Page(s):2 - 15  
Digital Object Identifier 10.1109/90.836474  
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- ☐ **1. RNS-based enhancements for direct digital frequency synthesis**  
Chren, W.A.;  
Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on [see also Circuits and Systems II: Express Briefs, IEEE Transactions on]  
Volume 42, Issue 8, Aug. 1995 Page(s):516 - 524  
Digital Object Identifier 10.1109/82.404073  
[AbstractPlus](#) | Full Text: [PDF\(712 KB\)](#) IEEE JNL
- ☐ **2. Circuit techniques in a 266-MHz MMX-enabled processor**  
Draper, D.; Crowley, M.; Holst, J.; Favor, G.; Schoy, A.; Trull, J.; Ben-Meir, A.; Khanna, R.; Wendell, D.; Krishna, R.; Nolan, J.; Mallick, D.; Partovi, H.; Roberts, M.; Johnson, M.; Lee, T.;  
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- ☐ **3. Design of a configurable accelerator for moment computation**  
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- ☐ **4. Itsy: stretching the bounds of mobile computing**  
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- ☐ 1. **The Transmogriifier-2: a 1 million gate rapid-prototyping system**  
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- ☐ 2. **IP validation for FPGAs using Hardware Object Technology™**  
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Slomka, F.; Dorfel, M.; Munzenberger, R.; Hofmann, R.;  
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- ☐ **14. Evolvable platform for array processing: a one-chip approach**  
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